Analog Design
Kevin Aylward B.Sc.
Low Voltage
Operational Amplifier Design
1 V, 0.35 ma, 45 nm, 90 dB, 100 MHz, 10 ns
Two Stage

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Overview

This paper presents an operational amplifier design example of a deep sub-micron, two stage, 1V, 0.35 ma operational amplifier with a nominal DC open loop gain of 90 dB and full power bandwidth of 100 MHz.

Introduction

Low voltage, high speed, amplifier design can be problematic, particular so at a 1V supply voltage. Achieving high DC gain and low static offset usually requires techniques not typically required at larger voltages. A key issue is the difficulty in using stacked cascode structures to obtain large DC gain due to the lack of voltage headroom for such structures. This issue is severely compounded due to the very low early voltage of the short gate lengths and their resulting low output resistance which produces a corresponding low gm.ro gain. Typically, V_a for 45nm gate lengths are less than 1V, compared to upwards of 20V-100V for longer gate devices. In principle, in a short gate length process it is possible to run longer gate lengths, however this impacts bandwidth significantly.

Design

A general consideration in any usual CMOS design is to always ensure that there is at least 100 mV of gate overdrive voltage, V_{gst}. This is to ensure respectable output resistance, gm and matching properties. Running significantly into sub-threshold impacts all of these properties. For a low voltage design this is quite difficult such that some compromises usually need to be made. What ultimately matters is whether or not the final desired specifications such as offset, loop gain and bandwidth are achieved, despite operating in some cases at non optimal conditions. For this design, for some worst case corners, V_{gst} is somewhat lower than desired, but nevertheless, key specifications are still achieved. For example, the worst case open loop gain is still 80 dB, with 10ns rise/fall times.

Two main features used to achieve high this DC gain and low static offset were:

1 Amplifier at the cascodes to boost the single cascode output impedance, and hence its gain.
2 Feedback around the output cascode to hold the cascode's V_{ds} at the same voltage, and hence matching.
V_{ds} operating voltages of all devices are quite tight, with typical ones being shown on the schematic.

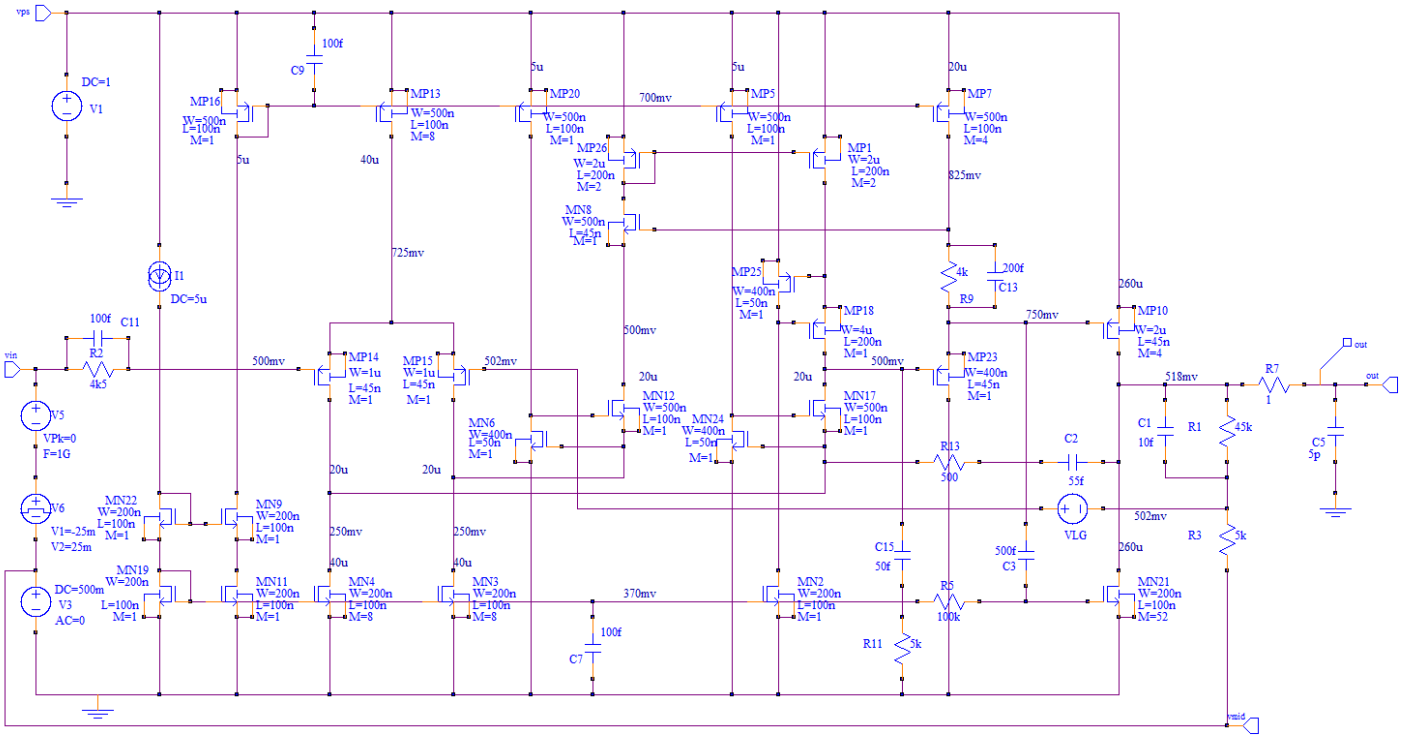
The design uses non-propriety device models from http://ptm.asu.edu/. These are models of a generic nature achievable at typical fab vendors. The specific models chosen had nominal threshold voltages of 250 mV. It should be noted that it is crucial that a process with such low threshold voltages is available. Worst case corner information was not available for the models so they were faked with what is known to be typical variations of such processes. All simulations were performed in SuperSpice, over temperatures of -40 degs to 125 degs.

Two main set-ups of the design were made. One for a closed loop gain of 20 dB and one for unity gain. Stability compensation was adjusted for each condition. Load was set at 5pf and 500ff.

The design is not fully optimised, being done from scratch in a couple of hours from topology invention to simulation. Its purpose is as a demonstration vehicle of what is potentially achievable for a two stage, 1V deep sub-micron op amp design.

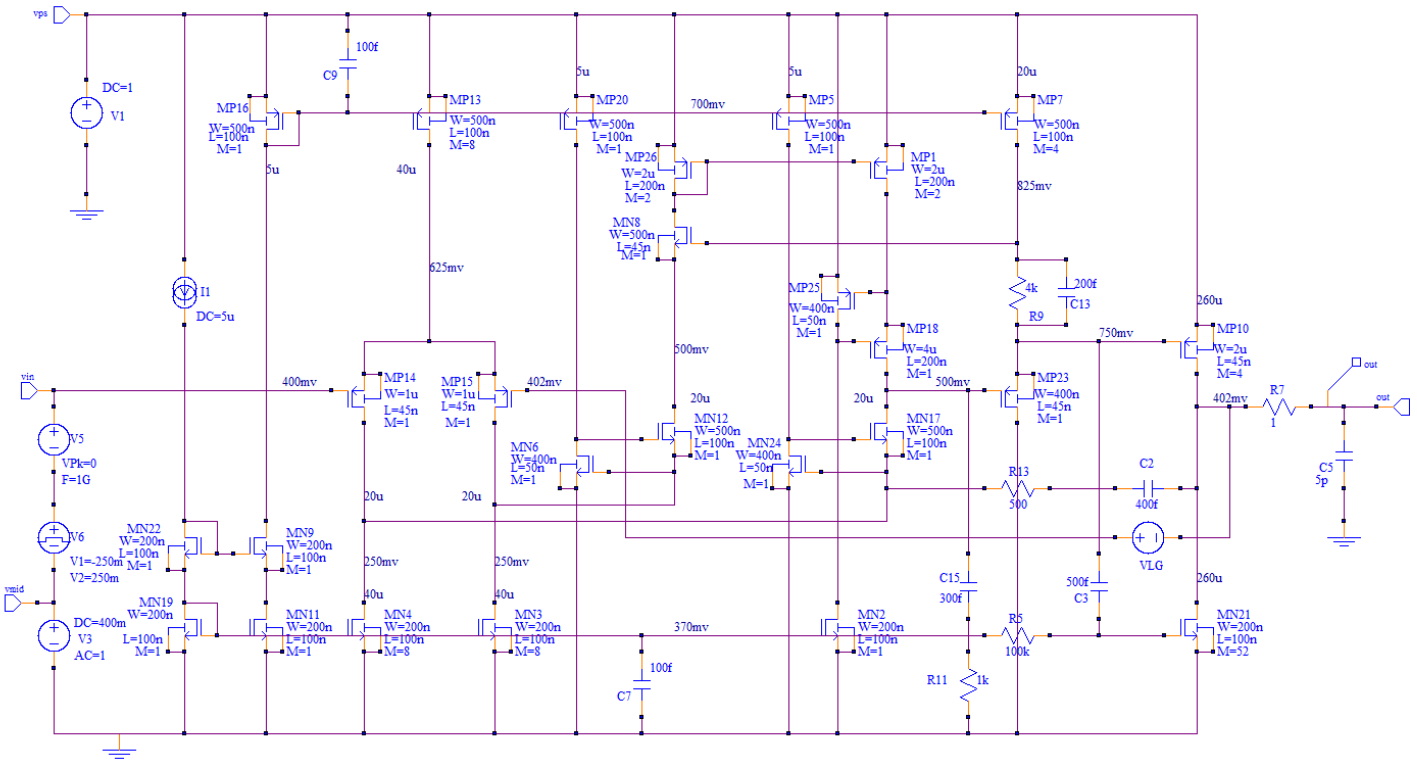
Schematic - 1 Volt 45 nm OpAmp, 20 dB Gain

Fig. 1



Schematic - 1 Volt 45 nm OpAmp, 0 dB Gain

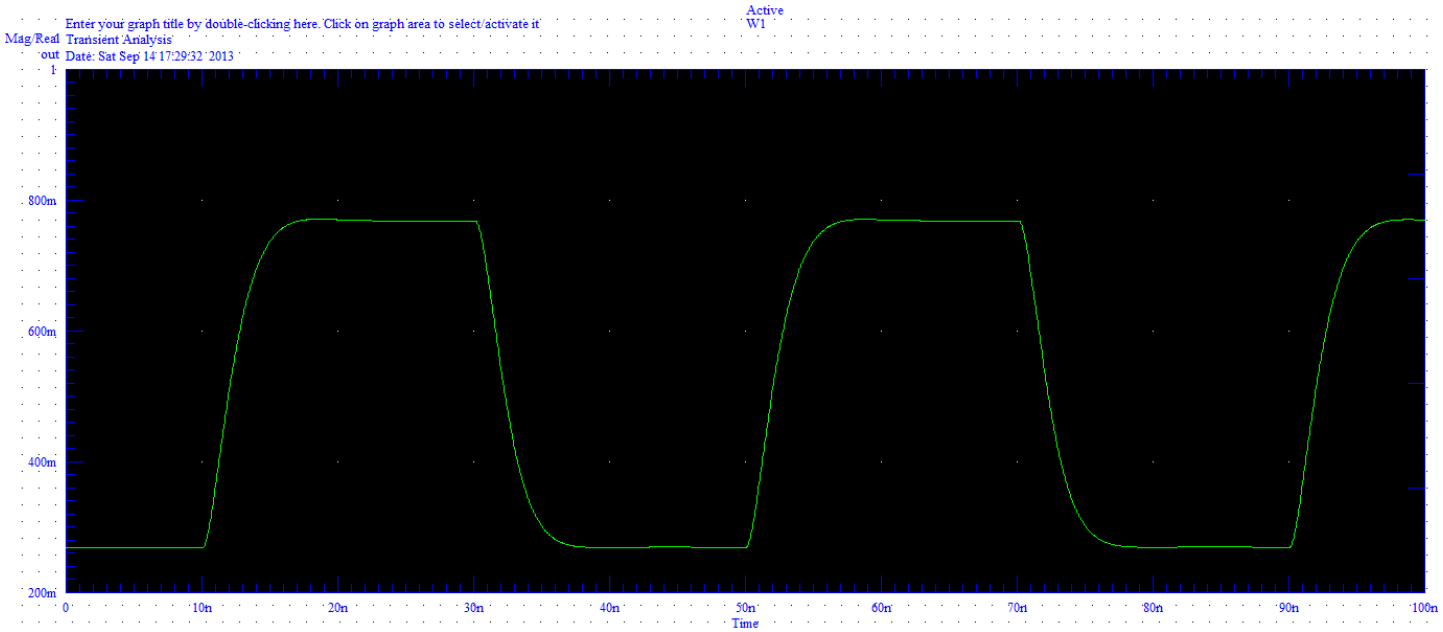
Fig. 2



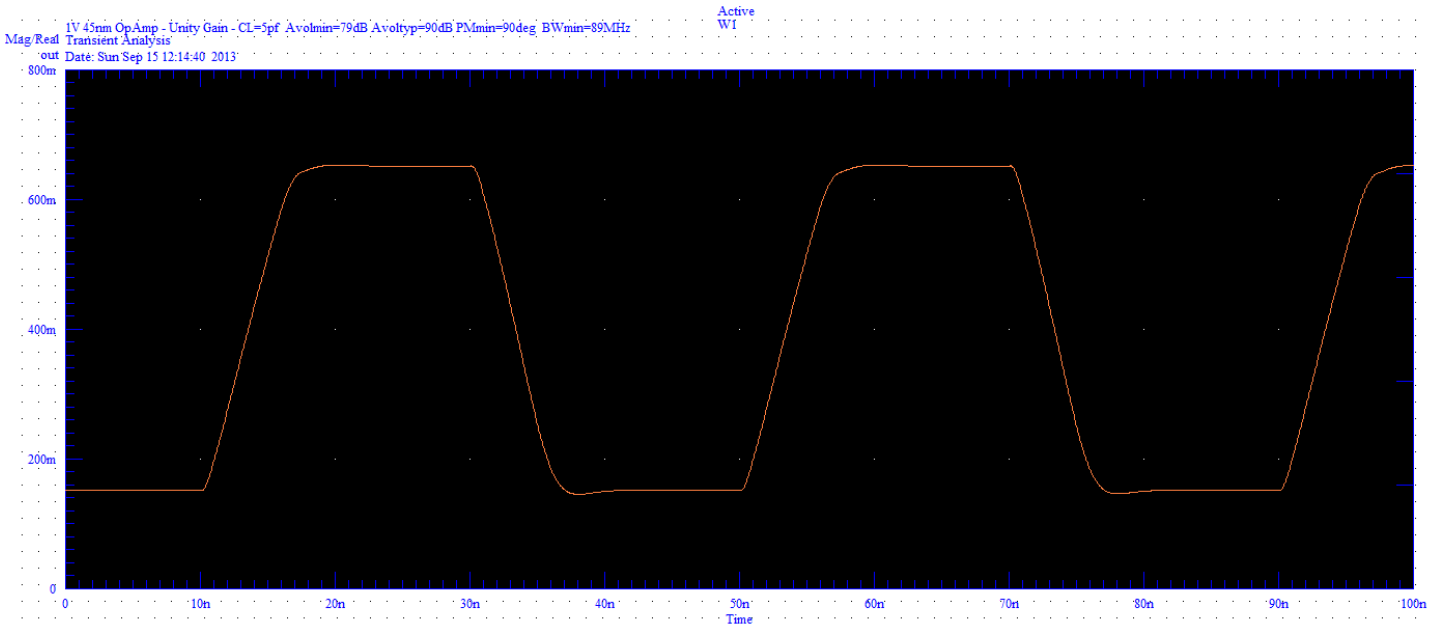
Typical Results

Topology	LG (dB)	F_{un}/BW (MHz)	PM (degs)	Static output offset mv	t_{rf} (ns)	t_{settle} (ns)	Power 1V (mW)	I_{vdd} (ma)	V_{cm} (V)
Avcl=20dB	70	100	70	18	5	10	0.35	0.35	0-0.4
Avcl=0dB	90	100	50	2	5	10	0.35	0.35	0-0.4

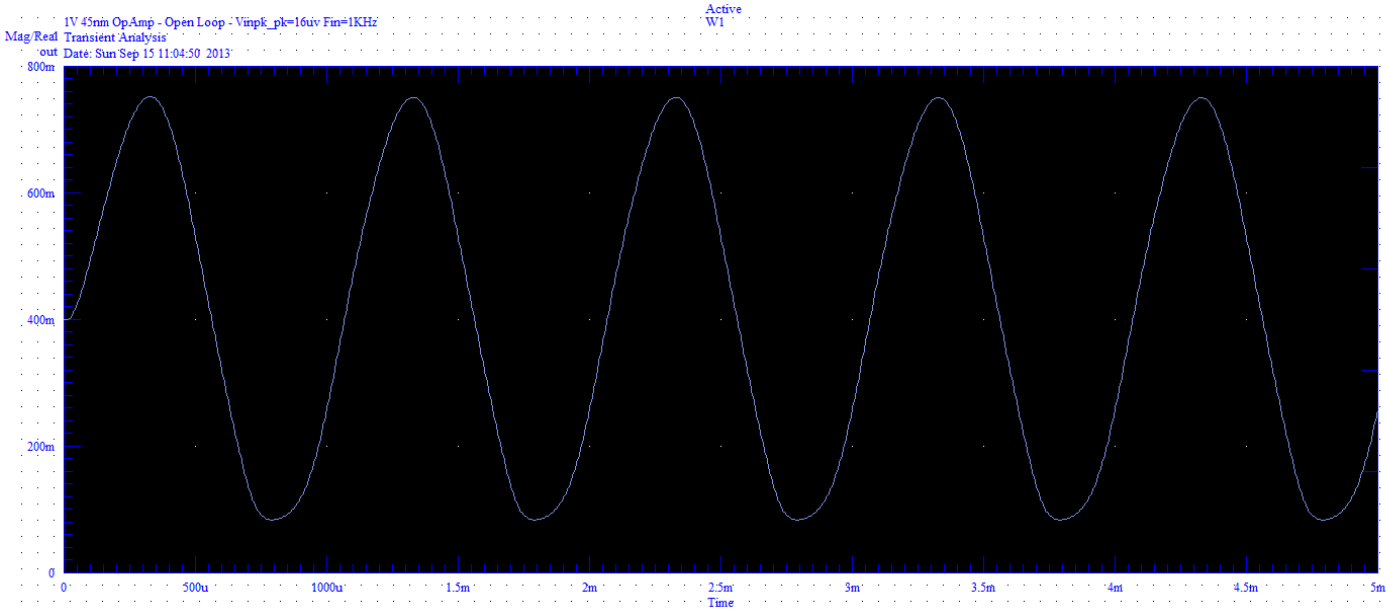
Nominal Transient – 20 dB Gain 25 mV Input, CL=5pf



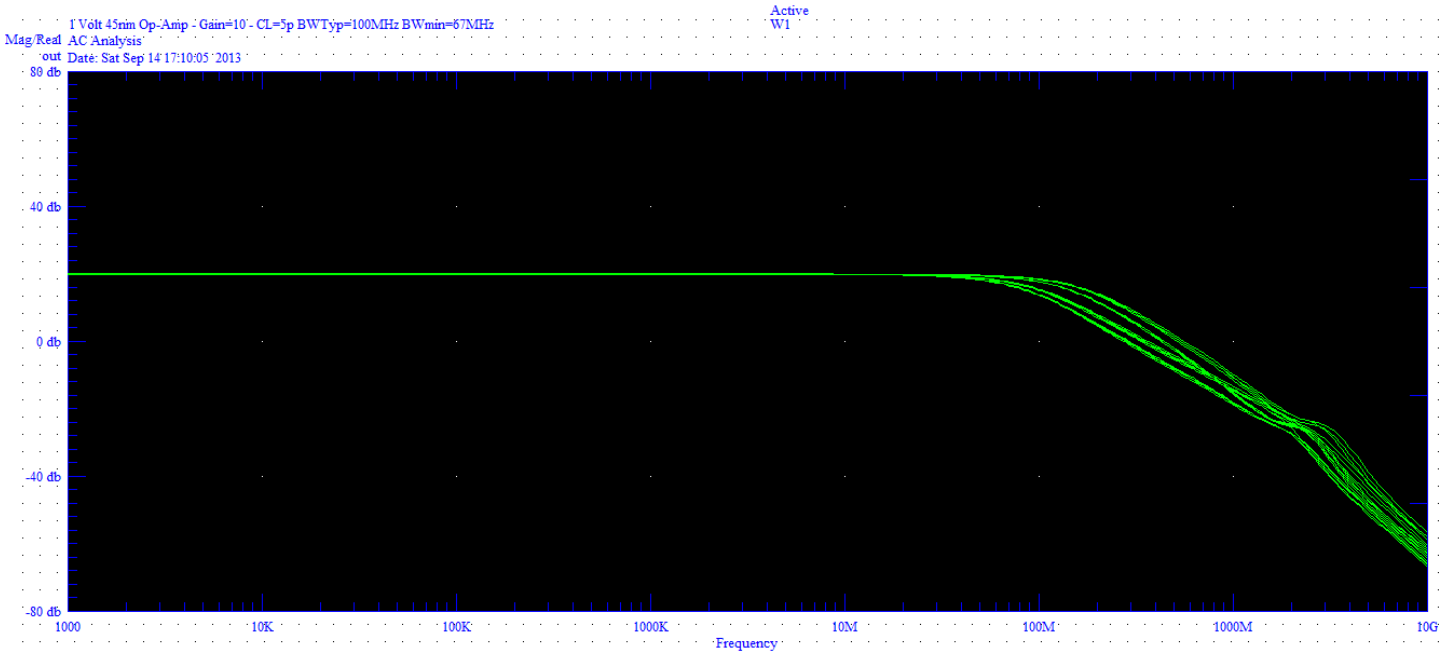
Nominal Transient – 0 dB Gain 250 mV Input, CL=5pf



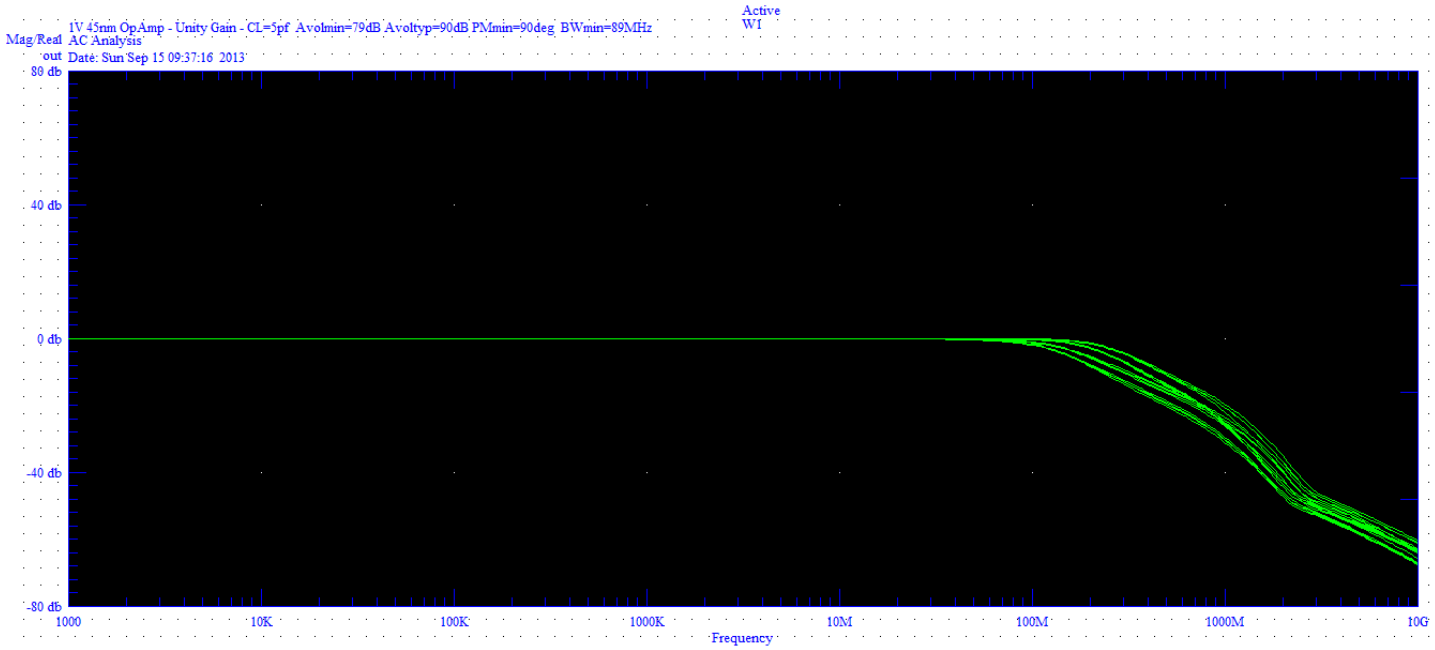
Nominal Transient – 8 uv Sine Input 1kHz Open Loop



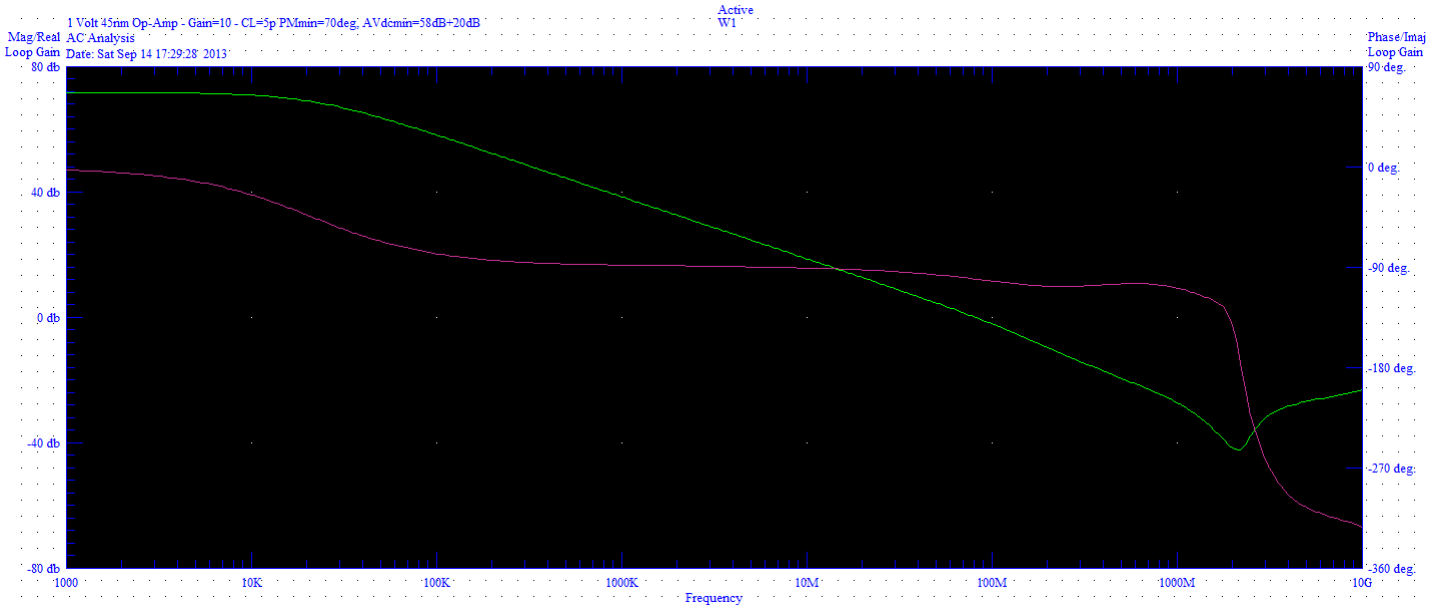
Worst Case Corners Frequency Response 20 dB Gain



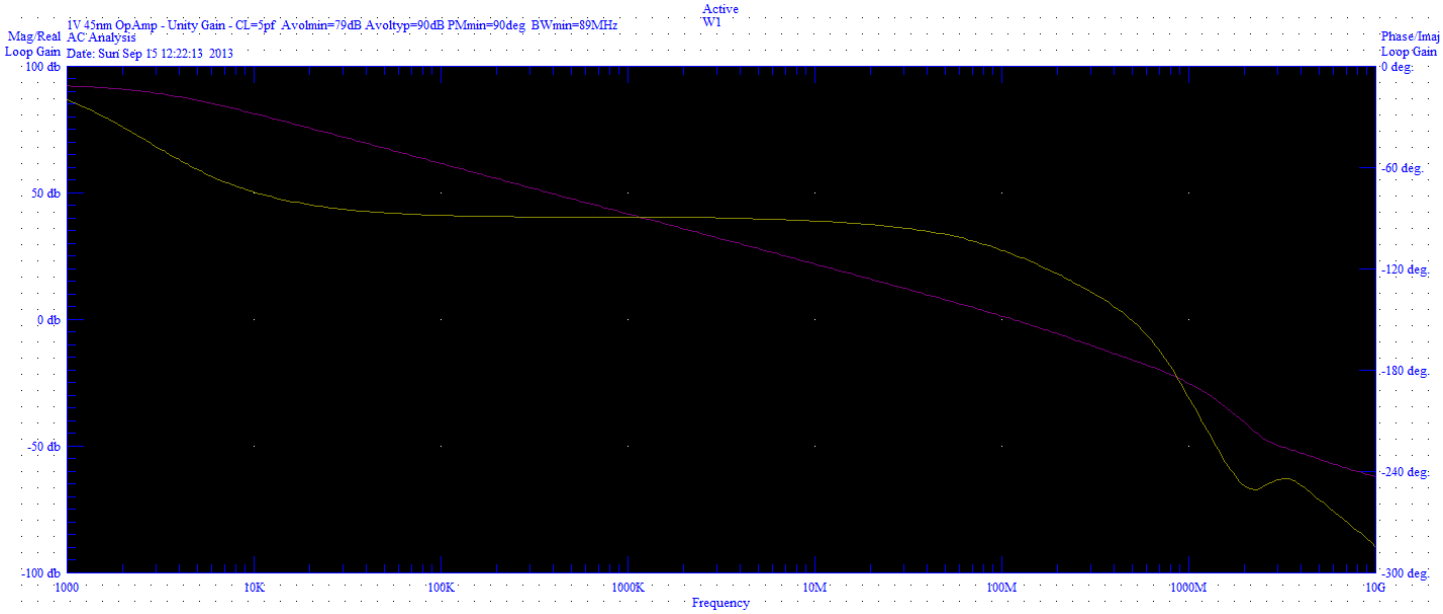
Worst Case Corners Frequency Response 0 dB Gain



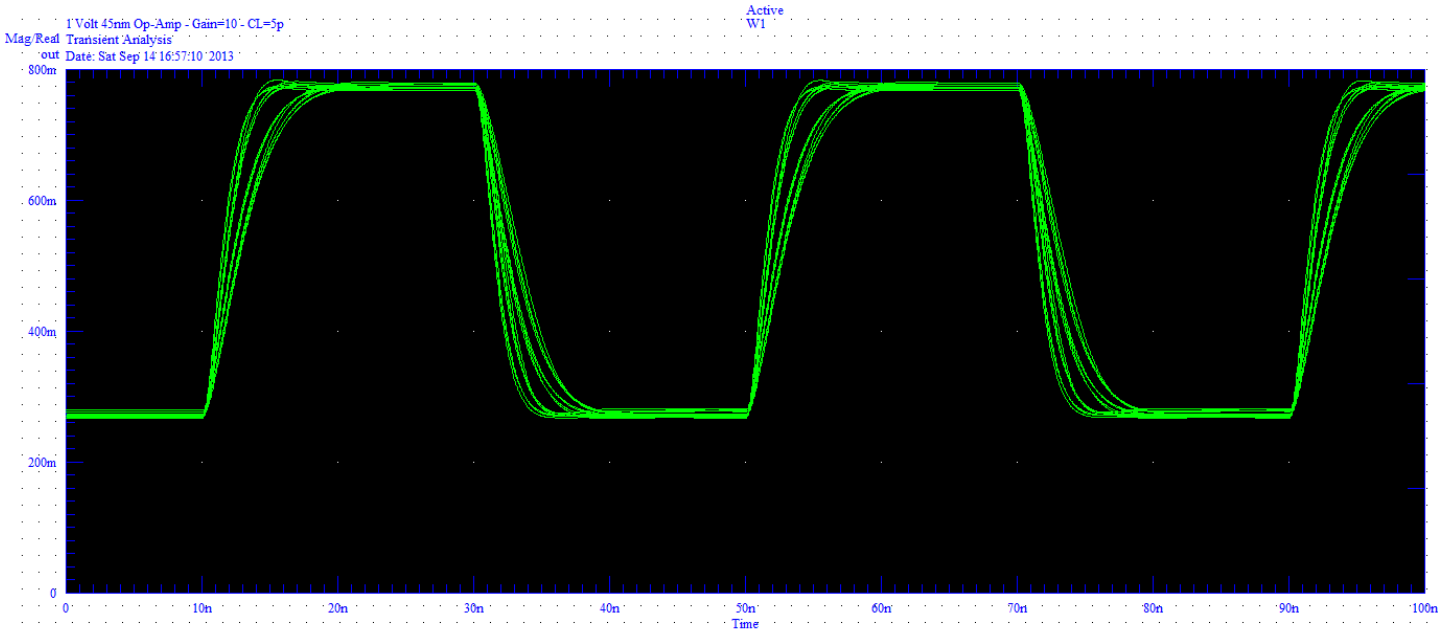
Nominal Loop Gain 20 dB Gain CL=5pf



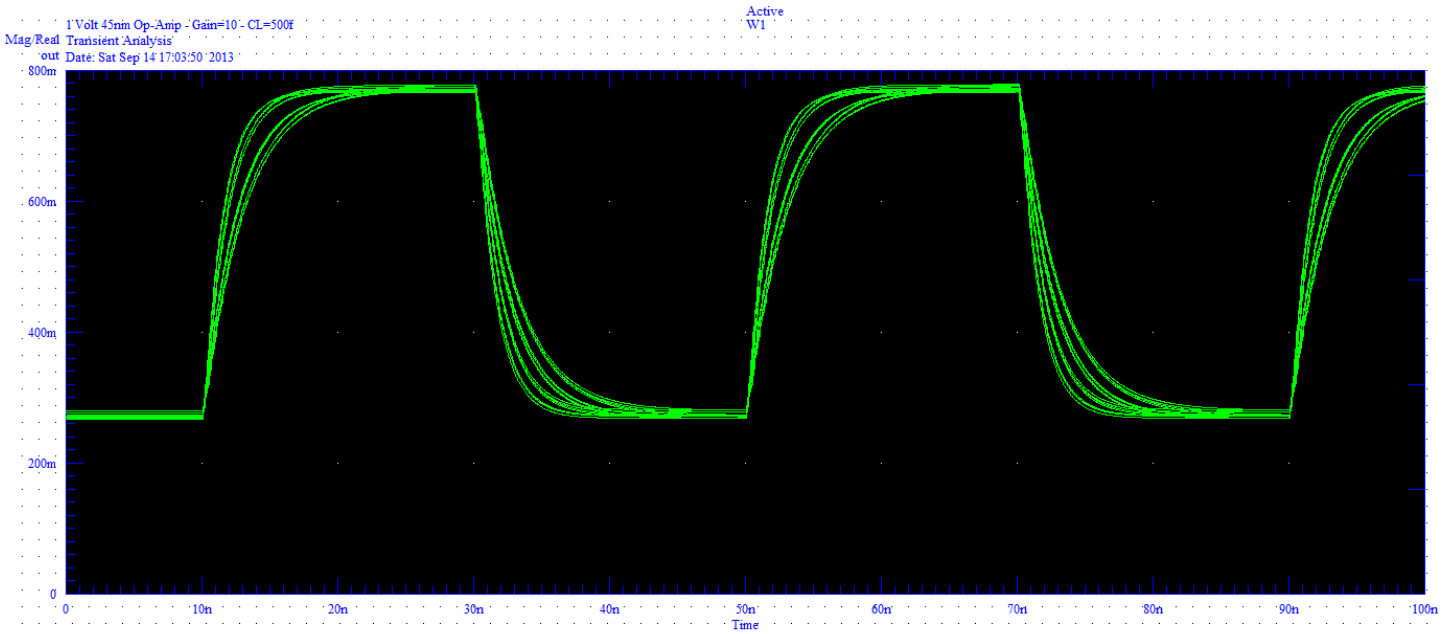
Nominal Loop Gain, 0 dB Gain CL=5pf



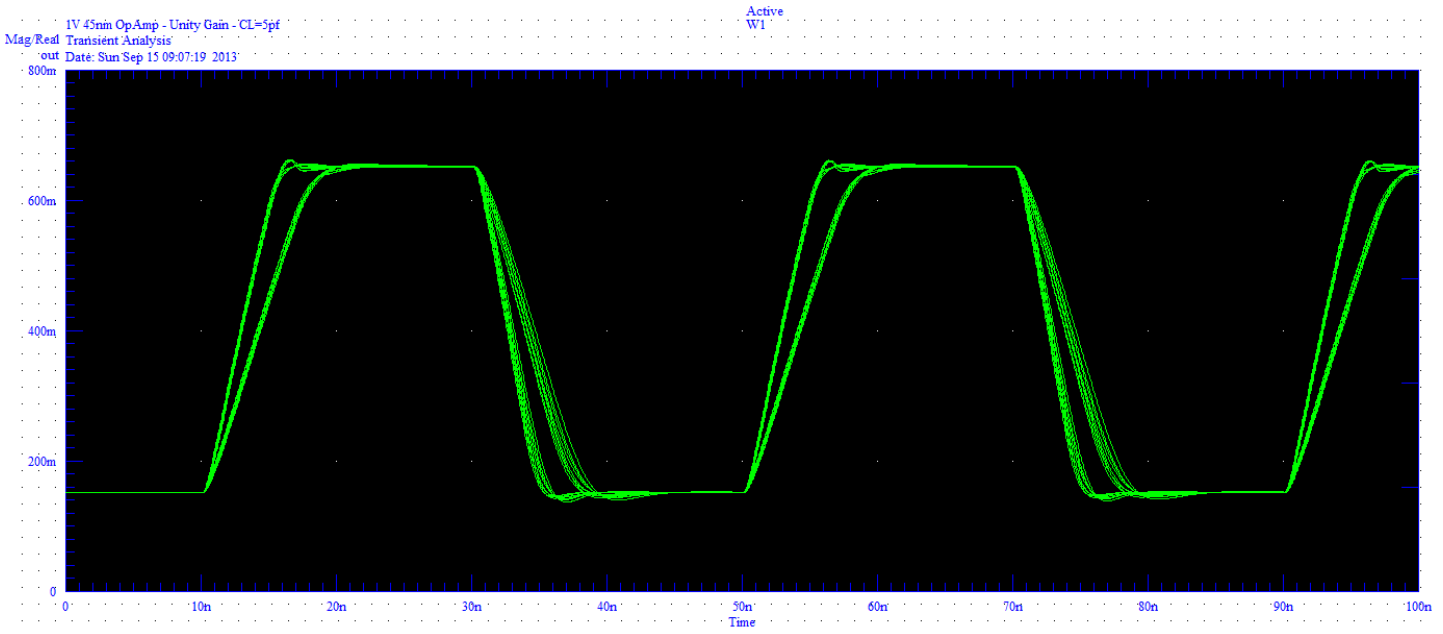
Worst Case Corners 20 dB Gain Transient CL=5pf



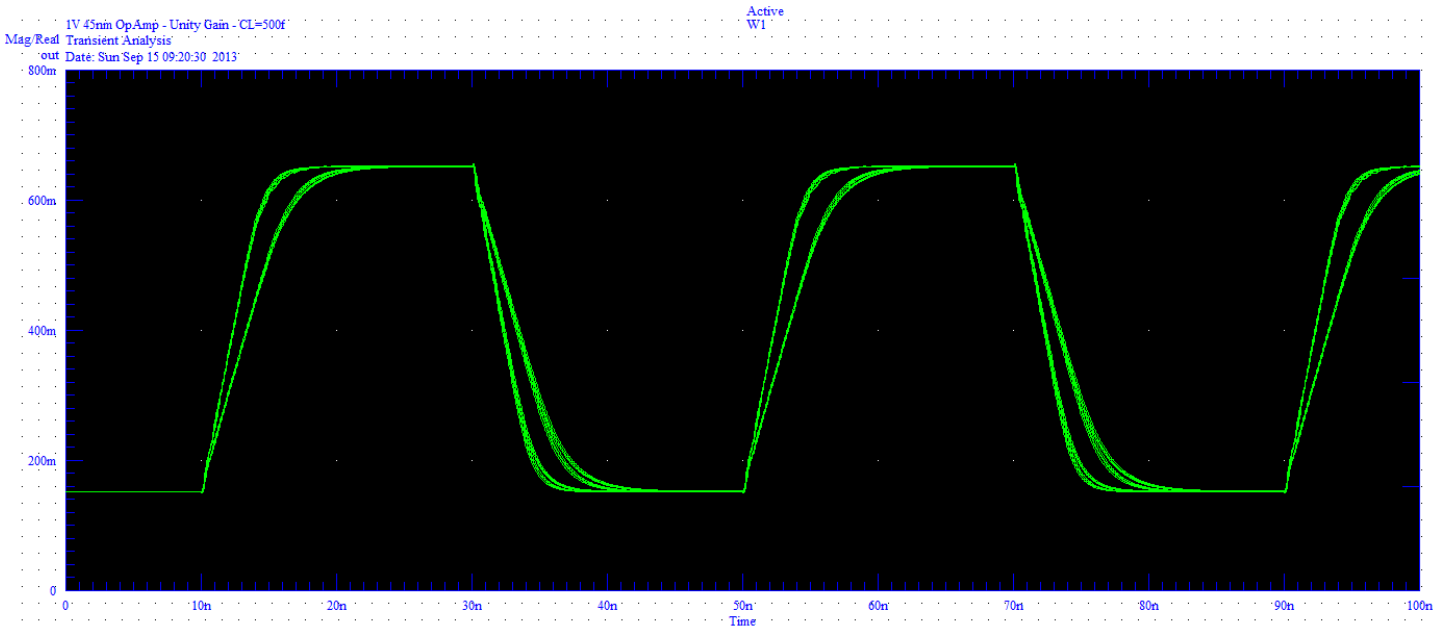
Worst Case Corners 20 dB Gain Transient CL=500ff



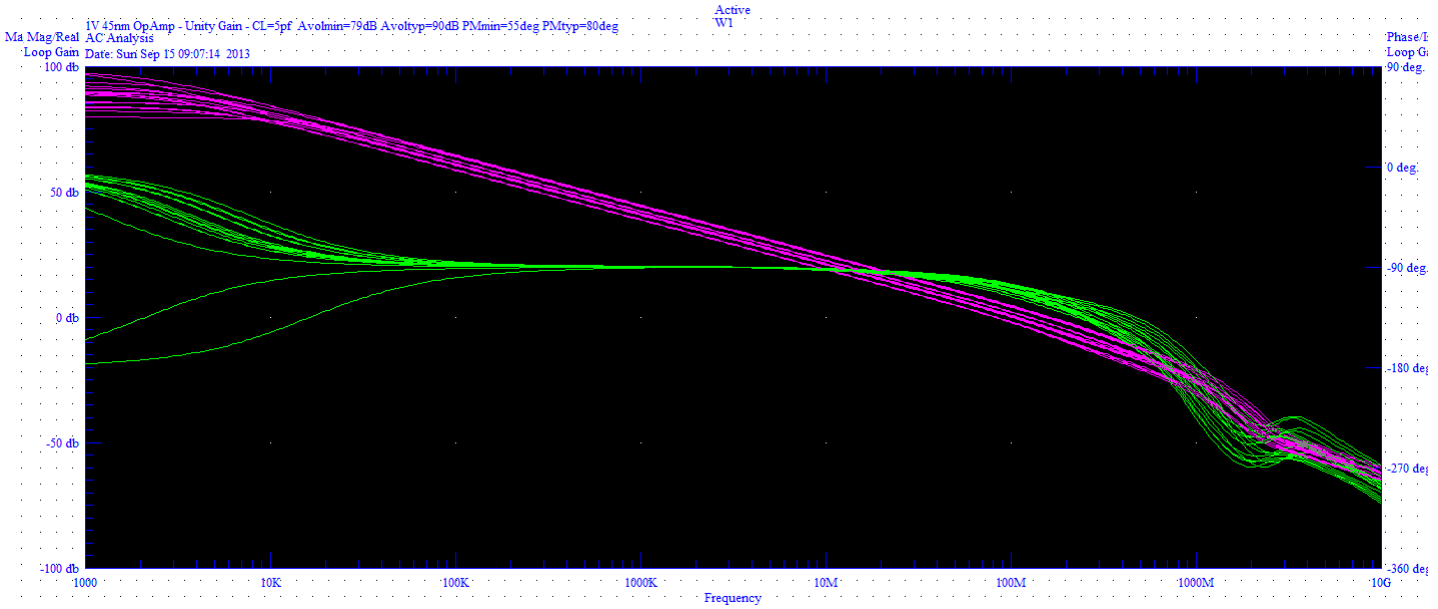
Worst Case Corners 0 dB Gain Transient CL=5pf



Worst Case Corners 0 dB Gain Transient CL=500ff



Worst Case Corners Loop Gain, 0 dB Gain CL=5pf



Summary

A 1 Volt deep sub-micron, two gain stage, operational amplifier has been presented with characteristics typically associated with a 3 stage design. The amplifier achieves its performance in two stages by careful choice of compensation, devices sizes and topology.

References

1 – “Analysis and Design of Analog Integrated Circuits” –Grey, Hurst, Lewis and Meyer
2 – “Design of Analog Integrated Circuits” – Behzal Razavi
3 – “CMOS Circuit Design, Layout, and Simulation” – Jackob R. Baker

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Website last modified 15th September 2013
www.kevinaylward.co.uk