Differential Oscillator

Kevin Aylward B.Sc.

Back to Phase Noise

Overview

Over the years, out of all possible oscillator topologies in integrated circuit design one general LC oscillator topology has been evolutionary selected as being, more or less optimum. This is the cross coupled LC oscillator. However, this standard topology also has a major blemish that has also been evolutionary copied, despite the fact that it is a less than optimum mutation.

Introduction

The cross coupled differential oscillator has shown itself to offer good performance. However, from the literature much effort has been expended in an effort to reduce the effect of up-converted 1/f noise generated by its tail current. This is essentially, misguided and a futile effort, principally caused by a misunderstanding of what is optimum for the system, not what might be optimum for the oscillator.

The design problem is to have a reasonable control over the operating current of the oscillator over supply voltages and process corners. This is solved by the current source but unfortunately can be the dominant source of 1/f phase noise around the oscillator frequency. It is not necessary, and unfortunately, does not actually solve the problem that the current source attempts to solve, that is, power supply rejection.

Typically, a high performance oscillator in a system may have its phase noise destroyed even by 100 uv of low frequency noise on the supply line, e.g. by an audio amplifier running off the same supply with voltages being dropped by common impedances. To eliminate this, high performance oscillators should to be ran of their own independent power supply. It is relatively straightforward to design such a power supply to have an 80 dB PSR, however, it is, essentially, impossible to do this for an oscillator directly.

The following shows an example topology that eliminates the current bias source, yet still has reasonable dc current stability

Topologies

Fig. 1

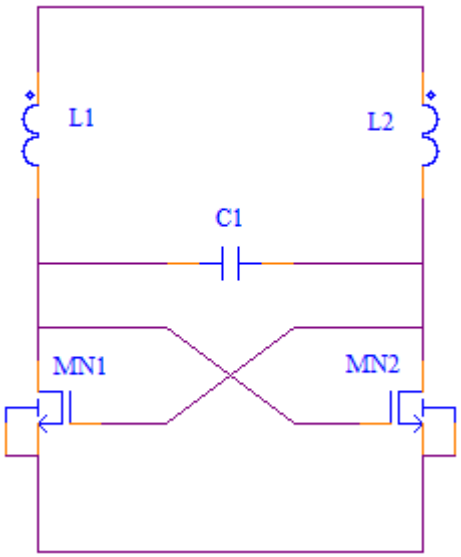
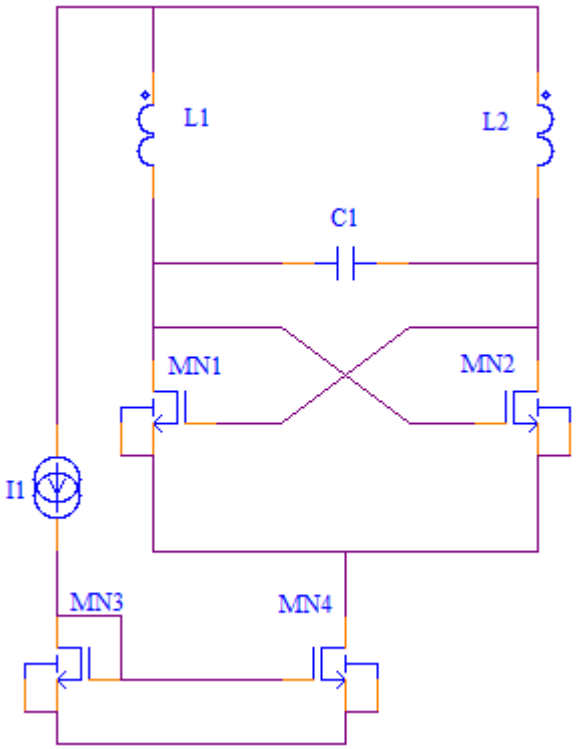


Fig. 1 is the standard differential oscillator topology. The issue with this circuit is that there is no defined operating current. It flaps in the wind based on the supply voltage and the gate threshold voltage. Quite possible a 10:1 variation in current, so not good news for a low power design.

Fig. 2



The Fig. 2 topology solves the undefined current problem, but adds noise from the current source. The current source noise is minimised when there is a 1:1 ratio of current to the input of the mirror and the mirror output, however this doubles the total supply current.

Fig. 3

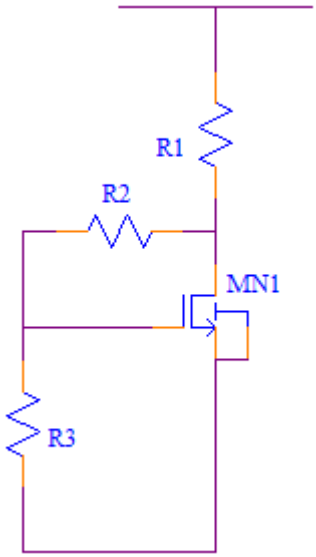
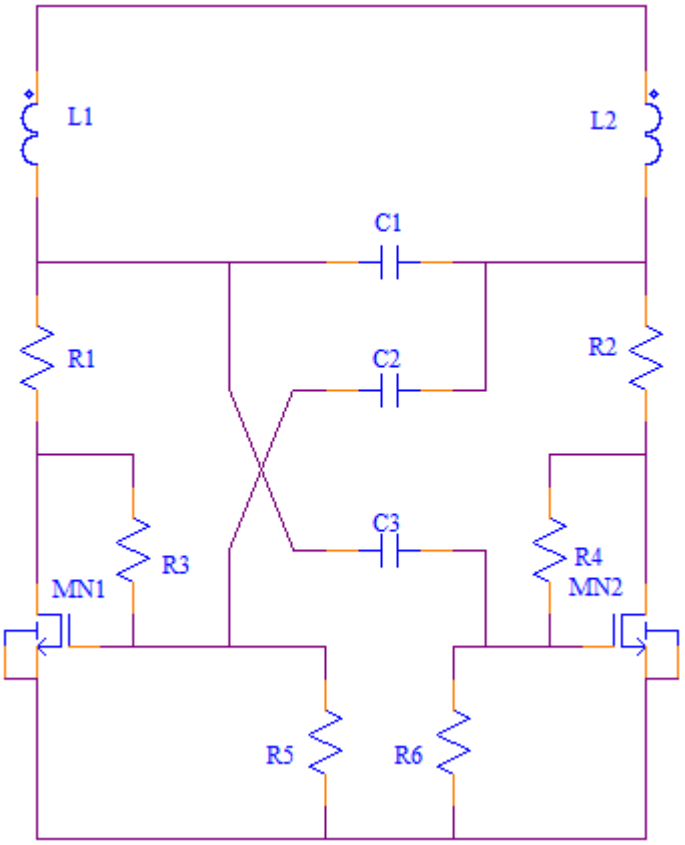


Fig. 3 illustrates a standard "V_{be} multiplier". MN1 is typically biased so that it runs with low V_{gst} and allows for its drain voltage to be multiplied up from round about its V_{th}. The drain current is thus set fairly accurately at the supply voltage minus Vd divided by R. Typically around 20% in operating current might be achieved.

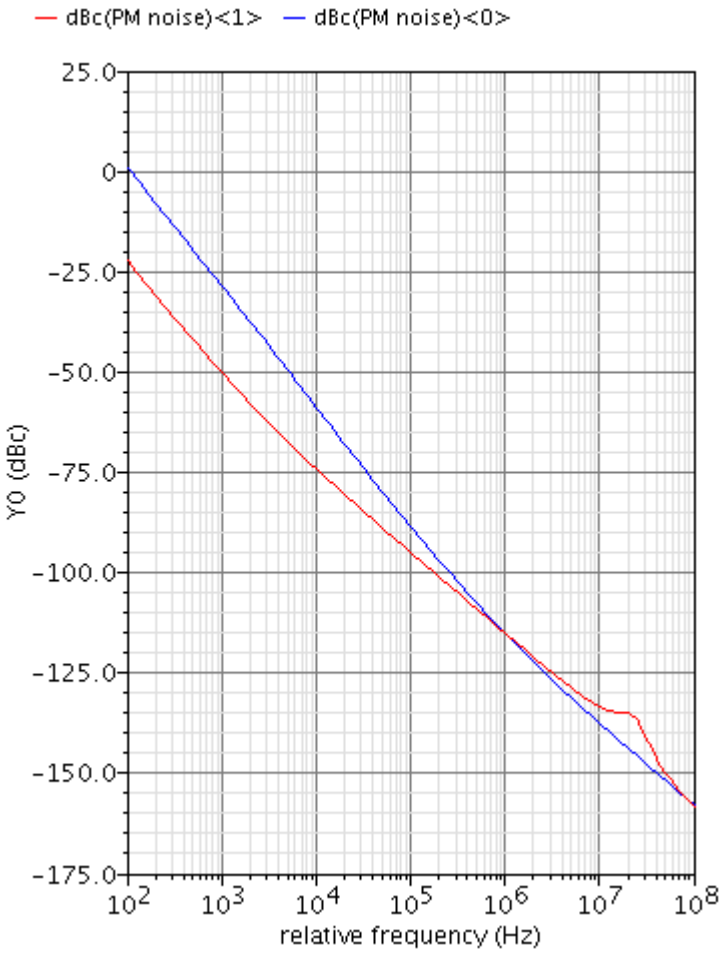
This topology may be used to bias up a differential oscillator as follows in Fig. 4

Fig. 4



The results for phase noise for Fig. 4 and its equivalent current sourced version, in a quickly knocked up test circuit are shown here in Fig. 5. Oscillation frequency is around 600 MHz. A main disadvantages of Fig. 4 is that there is less gain due to the drain resistors. However, what matters is whether there is enough gain and low enough flat-band noise for the application being considered.

Fig. 5



No prizes for guessing which trace is the tailed current source version.

© Kevin Aylward 2013
All rights reserved
The information on the page may be reproduced
providing that this source is acknowledged.
Website last modified 29th June 2013
www.kevinaylward.co.uk
