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# Analog Design

## Kevin Aylward B.Sc.

### Low Noise (RF) Amplifier

#### LNA Design

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### Overview

A reference LNA (low noise RF amplifier) topology, due to Professor Behzad Razavi, UCLA, is compared to an alternative topology via [SuperSpice](#) simulation.

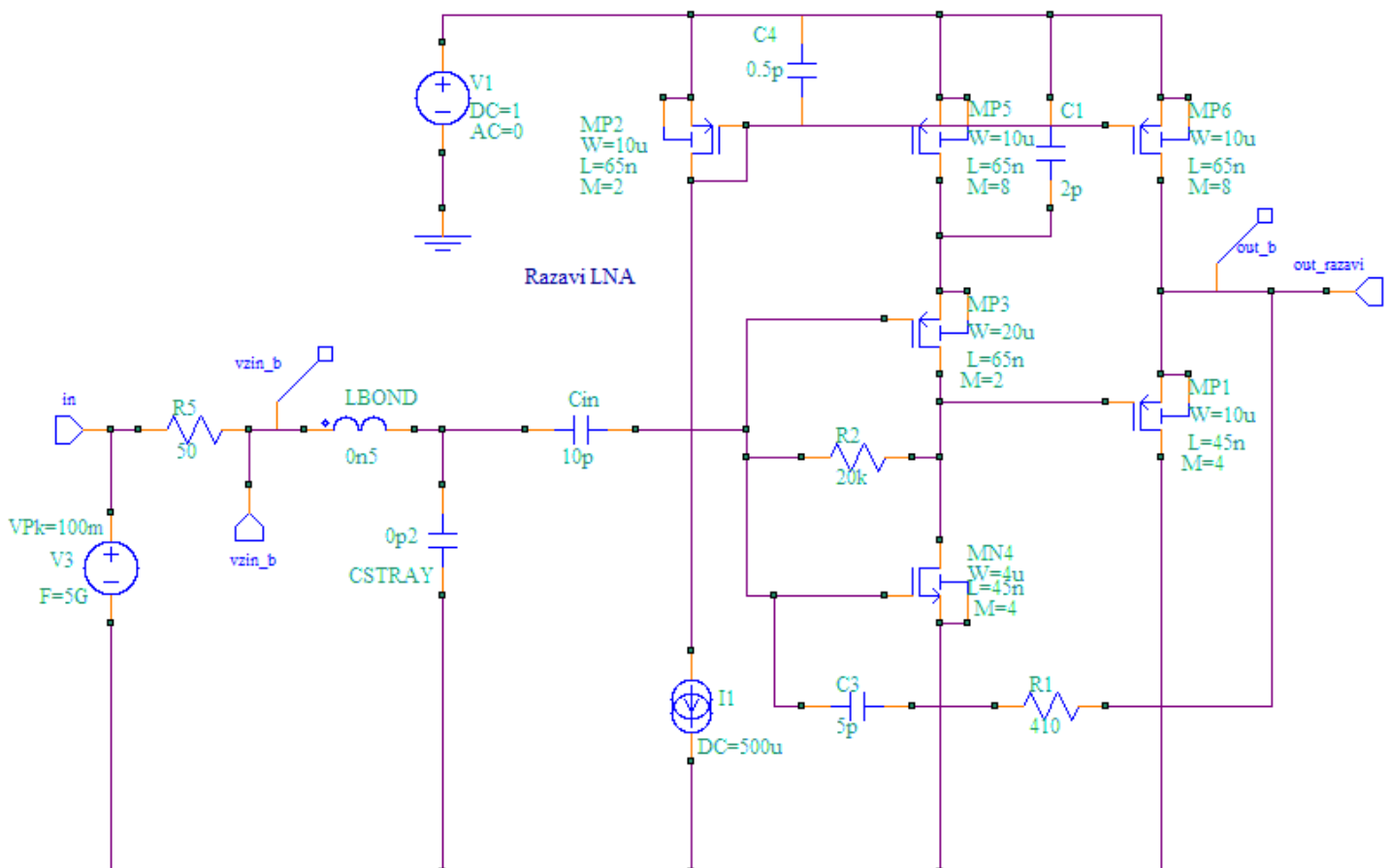
The design problem of a R.F LNA is usually, to obtain a low noise amplifier, with high gain, with large output swing, with a constant resistive input impedance, typically 50 ohms or 75 ohms, and with a high operating frequency and bandwidth, typically in the several GHz range. The design described here targets a 10 GHz 3dB BW.

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### Schematics

A nominal schematic topology, from Razavi's "RF Microelectronics" is shown as follows:

**Fig. 1 – Razavi Schematic**



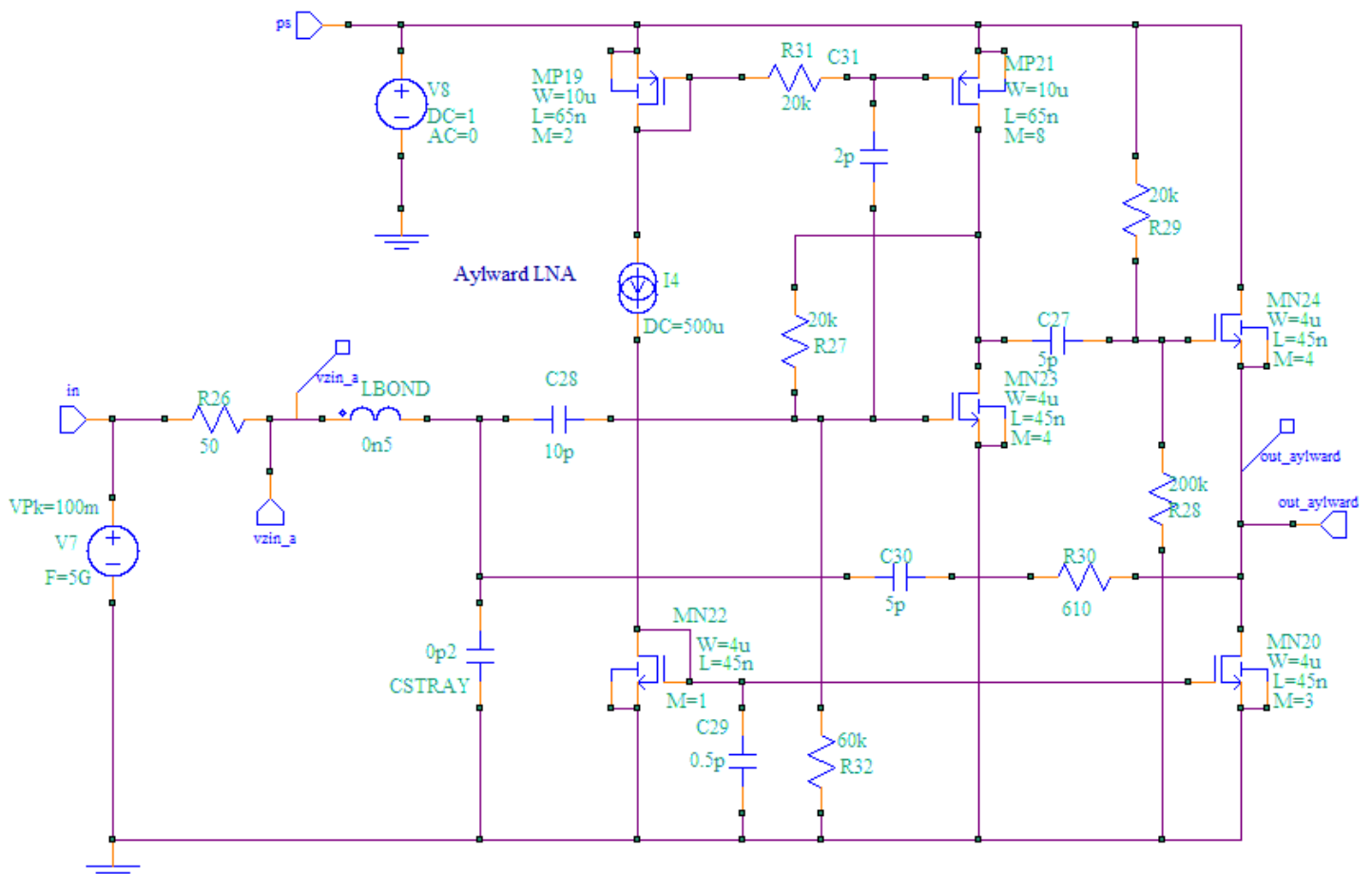
To perform the simulations, device models and sizes were selected that would be representative of a real design. The mosfet models chosen for design were non-proprietary device models from <http://ptm.asu.edu/>, representative of a 45nm process.

The principle design procedure being to chose a value for the feedback resistor that achieves a flatband 6dB attenuation at the amplifier input with zero phase shift, directly after the source input resistor. What ever gain is obtained is what it is! In the above schematic, LBOND and CSTRAY are nominal values chosen to represent ASIC parasitics. These may be significantly different in a real design. Simulations with different values of  $C_{in}$  were also performed.

By inspection, the following blemishes are immediately obvious with the Razavi topology.

- 1 Reduced output headroom due to the direct coupling of the gain stage to its pmos source follower buffer.
- 2 Use of a slower pmos device rather than an nmos as the buffer.
- 3 The bias current source injects noise into the amplifier, requiring mitigation by a noise filtering capacitor
- 4 The feedback does not include  $C_{in}$ , causing additional source mismatch at lower frequencies.

**Fig. 2 – Aylward Schematic**



The following points are made with respect to the Fig.2 topology:

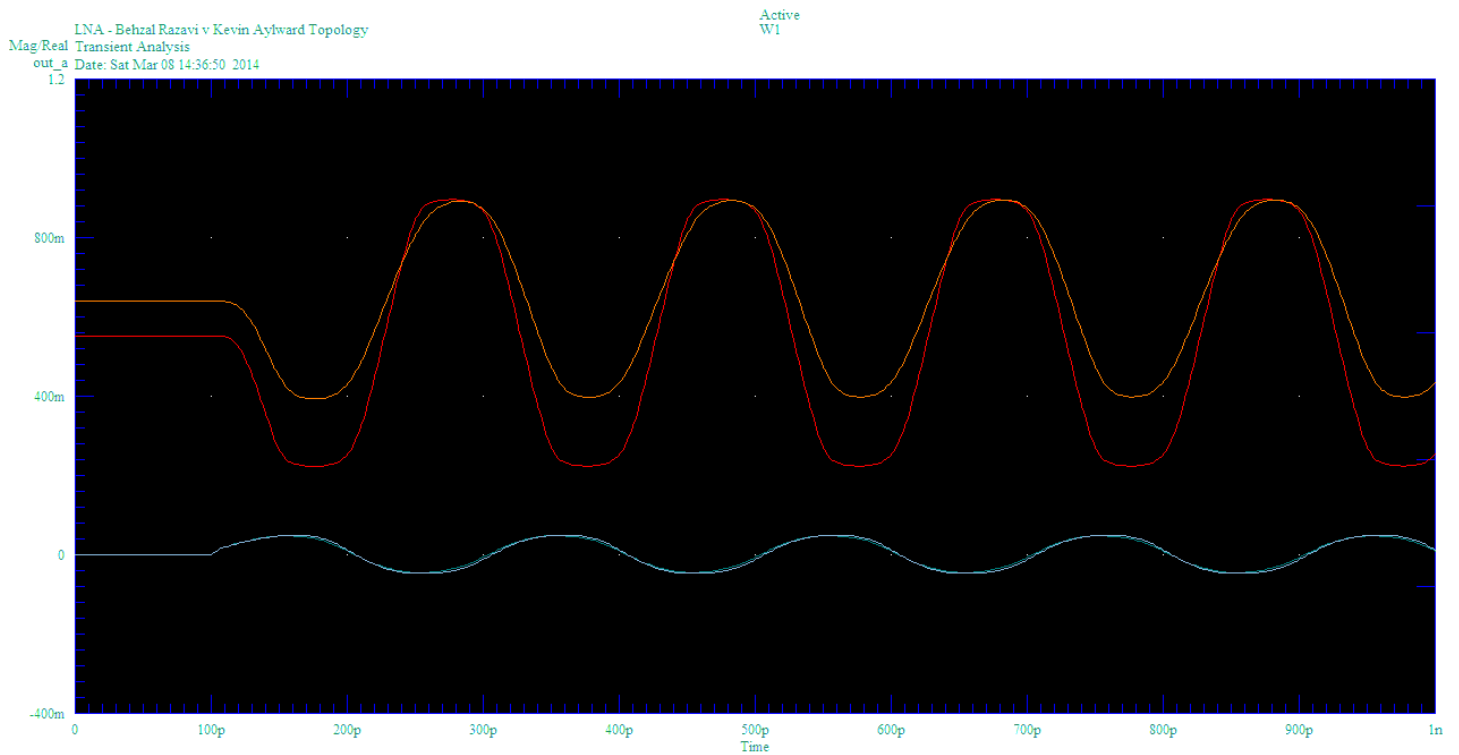
- 1 The output buffer is AC coupled, with its bias point being such that its gate input may go above the supply, allowing for a larger final output swing. This is achieved without the device voltage ratings being exceeded.
- 2 The output buffer is a faster, smaller nmos device.

- 3 Reduction of the dual push pull output and current determining devices to a single push pull device. This is achieved by AC coupling the input to the bias source making it serve both functions.
- 4 Inclusion of the input blocking capacitor within the feedback path.

### **Results Table**

| Topology                             | Aylward   | Razavi    | Units   |
|--------------------------------------|-----------|-----------|---------|
| Gain                                 | 14.3      | 10.6      | dB      |
| Bandwidth                            | 10        | 8.7       | GHz     |
| Gain Bandwidth Product               | 51.9      | 29.4      | GHz     |
| Output Swing                         | 0.67      | 0.49      | V       |
| Equivalent Input Noise               | 1.14      | 1.25      | nV/rtHz |
| N.F.                                 | 2.15      | 2.95      | dB      |
| Zin MAG Match BW<br>(+/- 1dB)        | 0.1 – 6.5 | 0.5 – 6.5 | GHz     |
| Zin Phase Match BW<br>(+/- 10 Degs.) | 0.2 - 11  | 1 - 11    | GHz     |
|                                      |           |           |         |

**Fig. 3 – Output Swing**

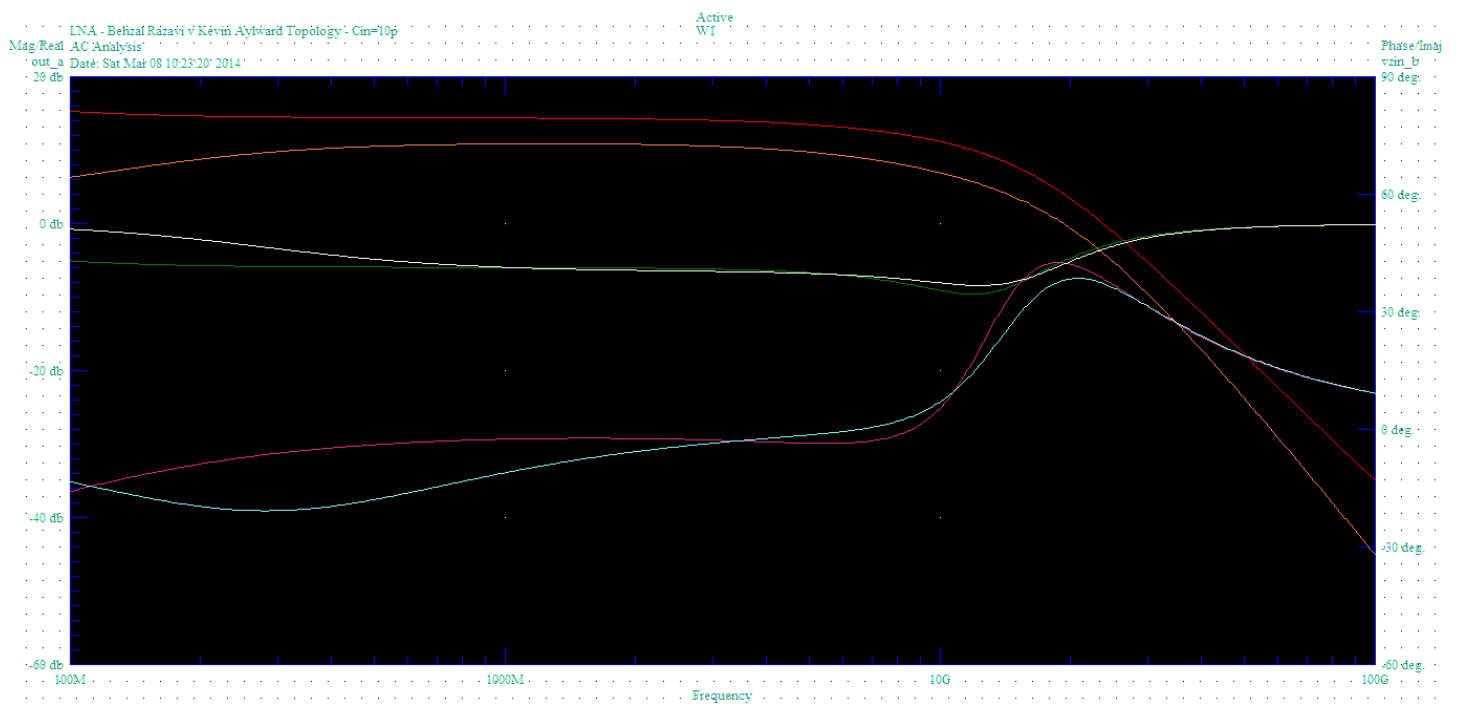


Orange – Razavi topology, output

Red – Aylward topology, output

Green and violet, inputs.

**Fig. 4 – Bandwidth –  $C_{in}=10p$**



Orange – Razavi topology, output

Red – Aylward topology, output

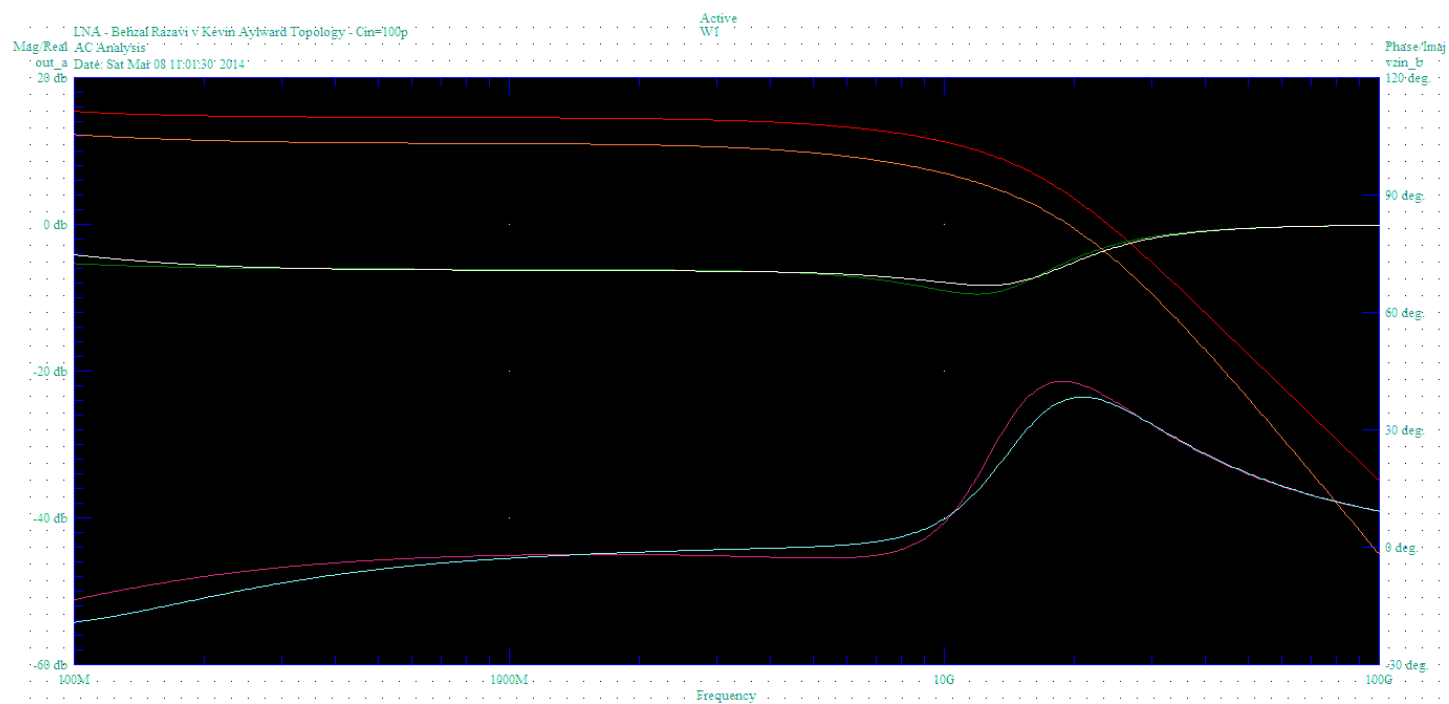
White – Razavi topology, input magnitude

Green – Aylward topology, input magnitude

Light Blue – Razavi topology, input phase

Pink – Aylward topology, input phase

**Fig. 5 – Bandwidth –  $C_{in}=100p$**



Orange – Razavi topology, output

Red – Aylward topology, output

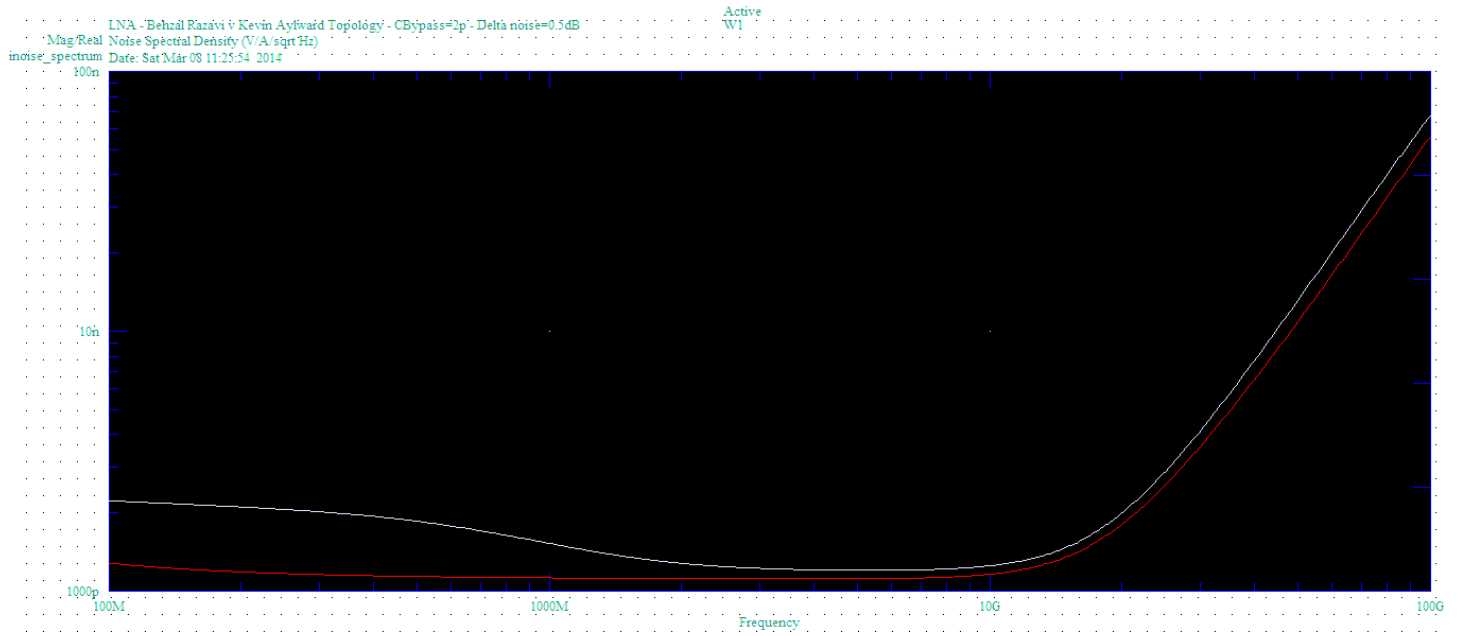
White – Razavi topology, input magnitude

Green – Aylward topology, input magnitude

Blue – Razavi topology, input phase

Pink – Aylward topology, input phase

**Fig. 6 – Input Noise – Cfilt=2p**

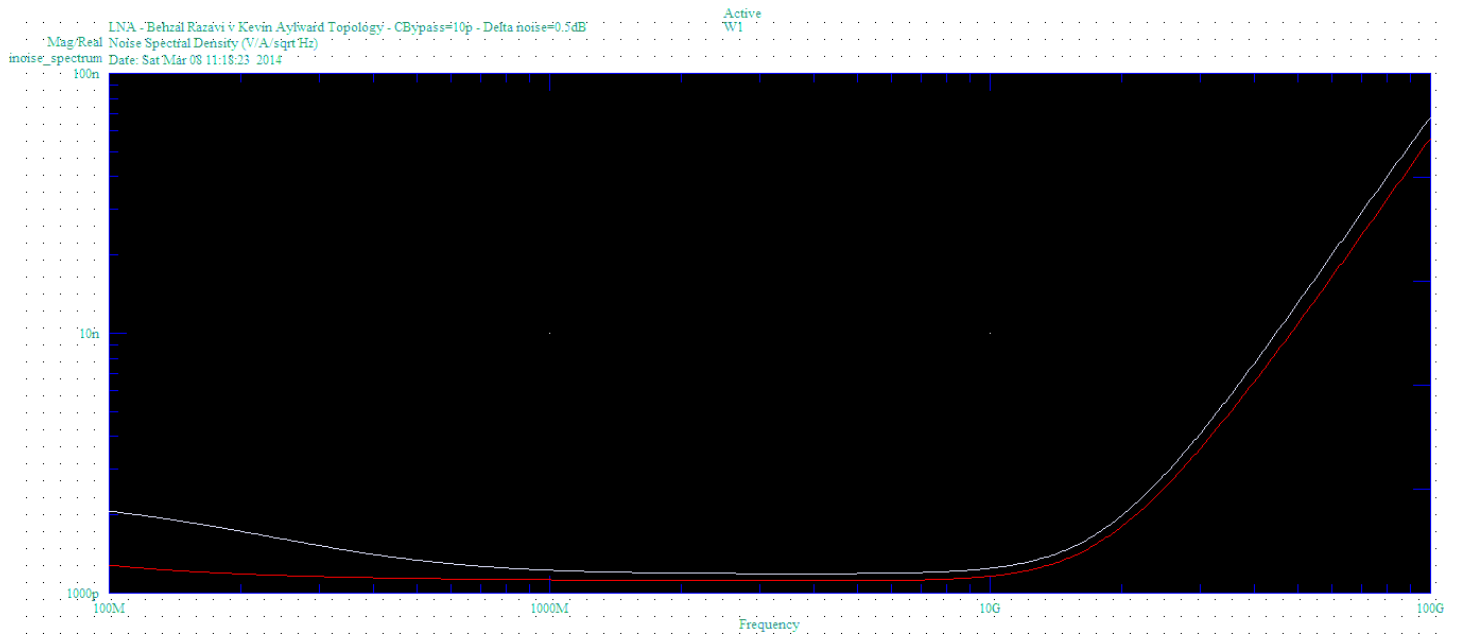


White - Razavi topology

Red – Aylward topology

Notes: Increase of noise at low frequencies for the Razavi topology due to its current source

**Fig. 7 – Input Noise – Cfilt=10p**



White - Razavi topology

Red – Aylward topology

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### **Summary**

A LNA topology has been presented that has superior performance in all key parameters, than a reference topology of Professor Behzad Razavi, UCLA, described in his instructional text book “RF Microelectronics”

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